REMARKS

New claims 13-30 have been added. Claims 1-30 are pending, with claims 1, 5, 9, 13, 19, and 25 being independent.

Submitted herewith are proposed corrections to Figs. 1, 5-6, 8-9, 12, 17-20, 22, 23A, 24, and 29. Upon approval of the proposed corrections and receipt of a Notice of Allowance, the drawings will be corrected in accordance with the procedure established therefor.

New claims 13, 15, 17-19, 21, 23-25, 27, and 29-30 respectively correspond to claims 1-12 in revised form, and new claims 14, 16, 20, 22, 26, and 28 recite further features of the present invention.

In the Office Action of October 4, 2000, claims 1-8 were rejected under 35 USC 102(a) as being anticipated by Hashimoto. Arguments traversing this rejection were presented on pages 12-18 of the request for reconsideration of March 5, 2001. Additional arguments traversing this rejection insofar as it may be deemed to be applicable to new claims 13, 15, 17-19, 21, and 23-24 respectively corresponding to claims 1-8 in revised form and to new claims 14, 16, 20, and 22 which recite further features of the present invention are presented below.

It is submitted that Hashimoto does not disclose the features of new claim 13 wherein the switching circuit includes a first transistor having an input, an output, and a gate electrode, the gate electrode of the first transistor

having a control voltage applied thereto, the control voltage being effective for turning the first transistor on and off, and a second transistor having an input, an output, and a gate electrode, the gate electrode of the second transistor having a bias voltage applied thereto, the input of the second transistor being connected to the output of the first transistor so that the first transistor and the second transistor are connected in series; or the features of new claim 15 wherein the bias voltage applied to the gate electrode of the second transistor is a first bias voltage, and wherein the first transistor and the second transistor are formed in a well layer having a second bias voltage applied thereto; or the features of new claim 17 wherein the switching circuit further includes a third transistor connected in parallel with the first transistor, wherein the first transistor and the second transistor are first conducting-type transistors, and wherein the third transistor is a second conducting-type transistor; or the features of new claim 18 wherein the first transistor and the second transistor are formed in a well layer, and wherein a voltage of the well layer is equal to a voltage of the input of the first transistor; or the features of new claim 19 wherein each of the first switching circuit and the second switching circuit includes a first transistor having an input, an output, and a gate electrode, the gate electrode of the first transistor having a control voltage applied thereto, the control voltage being effective for turning the first transistor on and off,

and a second transistor having an input, an output, and a gate electrode, the gate electrode of the second transistor having a bias voltage applied thereto, the input of the first transistor being connected to the input of the switching circuit, the input of the second transistor being connected to the output of the first transistor so that the first transistor and the second transistor are connected in series, and the output of the second transistor being connected to the output of the switching circuit; or the features of new claim 21 wherein the bias voltage applied to the gate electrode of the second transistor is a first bias voltage, and wherein the first transistor and the second transistor are formed in a well layer having a second bias voltage applied thereto; or the features of new claim 23 wherein each of the first switching circuit and the second switching circuit further includes a third transistor connected in parallel with the first transistor, wherein, in the first switching circuit, the first transistor and the second transistor are first conducting-type transistors, and the third transistor is a second conducting-type transistor, and wherein, in the second switching circuit, the first transistor and the second transistor are second conducting-type transistors, and the third transistor is a first conducting-type transistor; or the features of new claim 24 wherein the first transistor and the second transistor are formed in a well layer, and wherein a voltage of the well layer is equal to a voltage of the input of the first transistor, for substantially the same reasons

discussed on pages 12-18 of the request for reconsideration of March 5, 2001, that Hashimoto does not disclose or suggest the similar features of claims 1-8.

New claim 14 recites a liquid crystal display device according to claim 13, wherein the picture signal line driving circuit further includes a first amplifier circuit which applies an output voltage to the input of the first transistor, and a second amplifier circuit which applies an output voltage to the output of the second transistor, and wherein the following relationship is satisfied in the switching circuit when the first transistor is turned off: $|V1-V2|>|V4-V3|$, where V1 is a maximum voltage of the output voltage of the first amplifier circuit, V2 is a minimum voltage of the output voltage of the second amplifier circuit, V3 is the bias voltage applied to the gate electrode of the second transistor, and V4 is a voltage of the input of the first transistor. These features of new claim 14 are shown in the attached sketch which is based on Fig. 8 of the present application.

The switching circuit recited in claim 13 from which claim 14 depends may be considered to correspond, for example, to the combination of PMOS transistors PM1 and PM21 in Fig. 8, or the combination of NMOS transistors NM2 and NM22 in Fig. 8, or the combination of PMOS transistors PM2 and PM22 in Fig. 8, or the combination of NMOS transistors NM1 and NM21 in Fig. 8.

In the sketch, the combination of PMOS transistors PM1 and PM21 is shown as corresponding to the switching circuit,

with PMOS transistor PM1 corresponding to the first transistor of the switching circuit, and PMOS transistor PM21 corresponding to the second transistor of the switching circuit. Also, high-voltage amplifier circuit 271 is shown as corresponding to the first amplifier circuit recited in claim 14, and low-voltage amplifier circuit 272 is shown as corresponding to the second amplifier recited in claim 14.

As shown in the sketch, a bias voltage V3 of 0 V is applied to the gate electrode of second transistor PM21. As described, for example, on page 31, lines 1-18, of the substitute specification submitted with the preliminary amendment of March 8, 1999, when first transistor PM1 is turned off, the input voltage of second transistor PM21 is substantially equal to the bias voltage V3 applied to the gate electrode of second transistor PM21, and is thus substantially V3, i.e. 0 V, as shown in the sketch.

As shown in the sketch, the output voltage of first amplifier circuit 271 is applied to the input of first transistor PM1 and ranges from 2.5 V to 10 V, thus having a maximum voltage V1 of 10 V. Thus, a voltage V4 of the input of first transistor PM1 is equal to the output voltage of first amplifier circuit 271 and ranges from 2.5 V to 10 V, thus having a maximum voltage of 10 V.

Also, as shown in the sketch, the output voltage of second amplifier circuit 272 is applied to the output of second transistor PM21 and ranges from -5 V to 2.5 V, thus having a minimum voltage V2 of -5 V.

Thus, as recited in claim 14, the following relationship is satisfied in the switching circuit when first transistor PM1 is off:

$$|V1-V2|>|V4-V3|$$

In the sketch,

V1 = 10 V
V2 = -5 V
V3 = 0 V
V4 = 10 V (maximum)

and thus

$$|10-(-5)|>|10-0|$$

i.e.

$$|15|>|10|$$

such that the relationship $|V1-V2|>|V4-V3|$ recited in new claim 14 is satisfied.

It is submitted that Hashimoto does not disclose or suggest the features of new claim 14 wherein the picture signal line driving circuit further includes a first amplifier circuit which applies an output voltage to the input of the first transistor, and a second amplifier circuit which applies an output voltage to the output of the second transistor, and wherein the following relationship is satisfied in the switching circuit when the first transistor is turned off: $|V1-V2|>|V4-V3|$, where V1 is a maximum voltage of the output voltage of the first amplifier circuit, V2 is a minimum voltage of the output voltage of the second amplifier circuit, V3 is the bias voltage applied to the gate electrode of the second transistor, and V4 is a voltage of the input of the first transistor, or the similar features of new claim 20

wherein the picture signal line driving circuit further includes a first amplifier circuit which applies an output voltage to the first input terminal, and a second amplifier circuit which applies an output voltage to the second input terminal, and wherein the following relationship is satisfied in each of the first switching circuit and the second switching circuit when the first transistor is turned off: $|V1-V2|>|V4-V3|$, where V1 is a maximum voltage of the output voltage of the first amplifier circuit, V2 is a minimum voltage of the output voltage of the second amplifier circuit, V3 is the bias voltage applied to the gate electrode of the second transistor, and V4 is a voltage of the input of the first transistor.

Furthermore, it is submitted that Hashimoto does not disclose the feature of new claims 16 and 22 wherein the second bias voltage is different from the first bias voltage.

Since Hashimoto does not disclose the features of new claims 13-24 discussed above, it is submitted that new claims 13-24 patentably distinguish over Hashimoto in the sense of 35 USC 102(a), and an indication to that effect is respectfully requested.

In the Office Action of October 4, 2000, claims 9-12 were rejected under 35 USC 102(a) as being anticipated by Kitamura. Arguments traversing this rejection were presented on pages 18-24 of the request for reconsideration of March 5, 2001. Additional arguments traversing this rejection insofar as it may be deemed to be applicable to new claims 25, 27, and 29-30

respectively corresponding to claims 9-12 in revised form and to new claims 26 and 28 which recite further features of the present invention are presented below.

It is submitted that Kitamura does not disclose the features of new claim 25 wherein each of the first switching circuit, the second switching circuit, the third switching circuit, and the fourth switching circuit includes a first transistor having an input, an output, and a gate electrode, the gate electrode of the first transistor having a control voltage applied thereto, the control voltage being effective for turning the first transistor on and off, a second transistor having an input, an output, and a gate electrode, the gate electrode of the second transistor having a bias voltage applied thereto, the input of the first transistor being connected to the input of the switching circuit, the input of the second transistor being connected to the output of the first transistor so that the first transistor and the second transistor are connected in series, and the output of the second transistor being connected to the output of the switching circuit; or the features of new claim 27 wherein the bias voltage applied to the gate electrode of the second transistor is a first bias voltage, and wherein the first transistor and the second transistor are formed in a well layer having a second bias voltage applied thereto; or the features of new claim 29 wherein each of the first switching circuit, the second switching circuit, the third switching circuit, and the fourth switching circuit further includes a

third transistor connected in parallel with the first transistor, wherein, in the first switching circuit and the third switching circuit, the first transistor and the second transistor are first conducting-type transistors, and the third transistor is a second conducting-type transistor, and wherein, in the second switching circuit and the fourth switching circuit, the first transistor and the second transistor are second conducting-type transistors, and the third transistor is a first conducting-type transistor, for substantially the same reasons discussed on pages 18-24 of the request for reconsideration of March 5, 2001, that Kitamura does not disclose or suggest the similar features of claims 9-12.

Furthermore, it is submitted that Kitamura does not disclose the features of new claim 26 wherein the following relationship is satisfied in each of the first switching circuit, the second switching circuit, the third switching circuit, and the fourth switching circuit when the first transistor is turned off: $|V1-V2|>|V4-V3|$, where V1 is a maximum voltage of the output voltage of the first output circuit, V2 is a minimum voltage of the output voltage of the second output circuit, V3 is the bias voltage applied to the gate electrode of the second transistor, and V4 is a voltage of the input of the first transistor. These features of new claim 26 are similar to the features of new claim 14 discussed above.

Furthermore, it is submitted that Kitamura does not disclose the feature of new claim 28 wherein the second bias voltage is different from the first bias voltage.

Since Kitamura does not disclose the features of new claims 25-30 discussed above, it is submitted that new claims 25-30 patentably distinguish over Kitamura in the sense of 35 USC 102(a), and an indication to that effect is respectfully requested.

For the reasons set forth above and in the request for reconsideration of March 5, 2001, it is submitted that all of the Examiner's rejections have been overcome, and that the application is now in condition for allowance. Reconsideration of the application and an action of a favorable nature are respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (501.36642X00).

Respectfully submitted,

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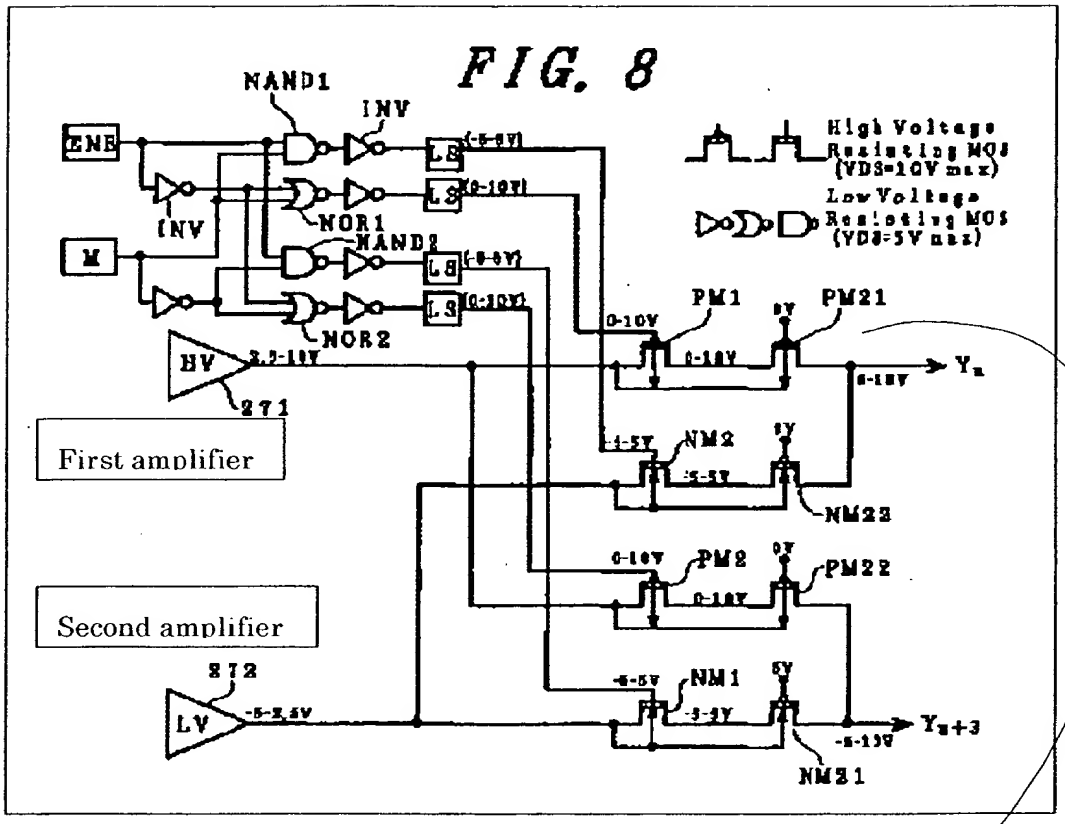
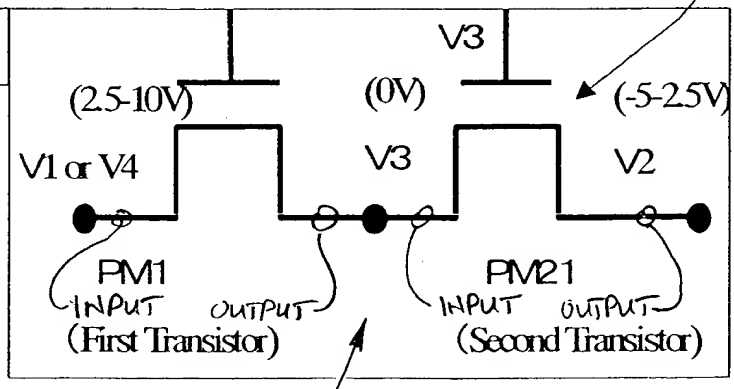
Attachment

SKETCH



Reference figure



WHEN FIRST TRANSISTOR IS OFF, VOLTAGE V3 OF INPUT OF SECOND TRANSISTOR IS SUBSTANTIALLY EQUAL TO BIAS VOLTAGE V3 APPLIED TO GATE ELECTRODE OF SECOND TRANSISTOR